NANEYE_GS

SPECIFICATION

PRELIMINARY

Project name	:	NANEYE_GS
Revision	:	2.0.02
Date	:	25/06/2012

Design house	:	AWAIBA GmbH
Contact Name	:	Stephan Voltz
Contact Address	:	Am Wegfeld
Contact Phone	:	+49 911 21521780
Contact E-mail	:	voltz@awaiba.com

1 History Record

Version	Date	Modifications	Author
1.0.01	19.04.2011	FRD update	Elena Reis
2.0.01	28.07.2011	Format update for release	M. Wäny
2.0.02	25.06.2012	Update package drawing	M. Wäny

2 Reference Documents

-

3 Contents

1 History Record....2
2 Reference Documents....3
3 Contents....4
4 Introduction....6
5 Disclaimer....7
6 General Statements and Conventions....8
6.1 Tolerances....8
6.2 Power supply....8
6.3 Clock specification....8
6.4 Digital Numbers....8
7 Block Diagram....9
8 External Components....10
9 Electrical Description....11
9.1 Absolute Maximum Ratings....11
9.2 Electrical overstress immunity....11
9.3 Operating Conditions....12
9.4 Electric Characteristics....12
9.4.1 LVDS OUTPUT....12
9.5 Optical Characteristics....13
10 Functional Description....14
10.1 General Sensor description....14
10.2 Interfaces....15
10.2.1 Serial Interface....15
10.2.2 Data interface....16
10.3 Sequence of operation....17
10.4 Timing characteristics....18
10.5 Data sequence and line transmission....19
10.6 Multi Sensor application scenarios....21
10.6.1 Option 1....21
10.6.2 Option 2....22
11 Control Interface....23
11.1.1 Serial Interface (I2C similar)....23
12 Pinout....25

12.1 Pads and Bond Pads position.....25
12.1.1 Pin Coordinates.....27

4 Introduction

NanEye_GS is a small form factor high sensitivity global shutter sensor with external trigger properties and frame rate up to 100Fps. The sensor features a high sensitivity global shutter pixel with 3.6um pitch. The global shutter property permits easy synchronization with external light sources or externally triggered events.

The sensors data Interface provides a bit serial LVDS data stream easy to receive in standard FPGA's or by standard deserializer components. The data output bus can be tristated in between the frame transfers to connect several devices on a dingle data bus.

The serial configuration interface is implemented similar to I2C interface, however with the possibility to connect multiple identical devices on a same bus.

The sensor main clock can be internally divided to accommodate lower data rate applications. The external sensor clock is provided over an LVDS differential link to avoid EMI/EMC issues even in case of remote sensor heads with extended connector lengths.

5 Disclaimer

The Integrated Circuit (IC) has been or will be designed and developed so as to conform in all material respects to the preceding introduced specification based on the performance indication and guideline from the silicon manufacturer regarding the target CMOS technology. Any change to the specification shall be mutually consulted and determined with the prior written consent of the parties. Any changes to the specifications required by the Customer shall be mutually agreed upon and laid down in writing as a supplement to or correction of the specifications.

AWAIBA does not warrant and Customer therefore expressly waives the existence of any parameters or features of the IC, which are not explicitly mentioned in the specification. It is the customer's responsibility and obligation to check compliance of the IC to the requirements of the application. The IC will not be designed for use as critical[1] component in medical, military or live sustaining [2] applications. Any use of the IC without prior written consent of AWAIBA in such applications is prohibited.

The above mentioned warranty is the only warranty given by AWAIBA. AWAIBA expressly disclaims all other warranties, whether expressed, implied, or statutory, including, without limitation, any implied or statutory warranties of merchantability, fitness for a particular purpose, and non-infringement, and any warranty that may arise by reason of usage of trade, custom or course of dealing, and customer hereby expressly waives any such warranties.

1) A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.
2) Life support devices, systems or applications are devices, systems or applications which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided, can be reasonably expected to result in a significant injury to the user.

6 General Statements and Conventions

Text in this document between "{ info only:" and "end info}" or "{" and "}" is for information only. Parameters and information given in this section contain background information . Performance and parameters given in these sections can not be guaranteed. No implicit nor explicit specification can be derived from these sections.

6.1 Tolerances

For all parameters, nominal value, upper, and lower bound of guaranteed specification are indicated. Parameters indicated without tolerances are for info only and can not be guaranteed.

6.2 Power supply

The lowest supply voltage in the chip is referred to as VSS. VSSxx indicates the lowest power supply voltage of a sub block xx of the circuit. All VSS power supply's have the same potential at all pins at any time. 0V is defined as being the voltage applied to the VSS pins.

The highest supply voltage of a sub block xx of the circuit is referred to as VDDxx. All pins carrying identical VDDxx power supply net labels have the same potential at any time, neglecting parasitic effects.

All voltage specifications are referred to VSS unless otherwise specified. All positive currents flow into a pin. The sinking of current means that current is flowing into a pin. The sourcing of current means that current is flowing out of a pin.

So far no detailed definition of the power supply is given. This will be worked out during the first pre design phase.

6.3 Clock specification

All timing information treated by a digital control part refers to the master clock frequency which is supplied on pin CLK, unless otherwise specified.

6.4 Digital Numbers

When ever referred to the output signal this is indicated in DN (Digital Numbers) equalling 1 unit (1LSB) of the on chip ADC. This quantity is sometimes also referred to as "grey levels".

7 Block Diagram

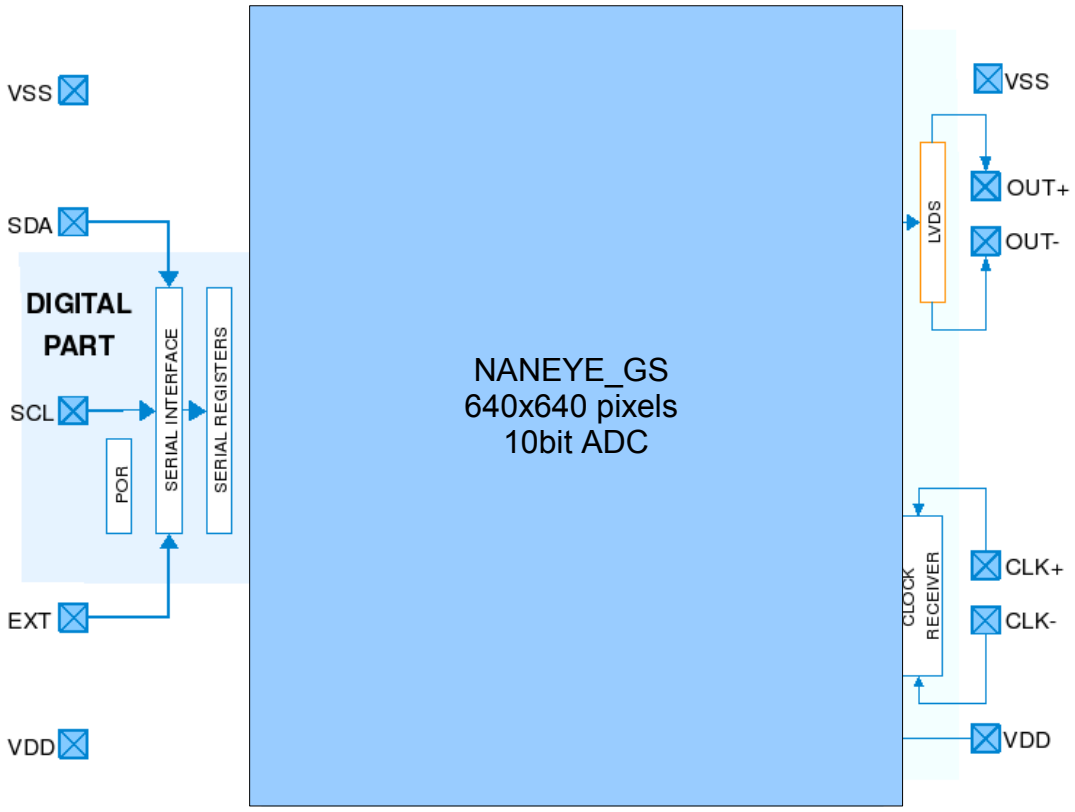

Figure 1: NANEYE_GS block diagram

8 External Components

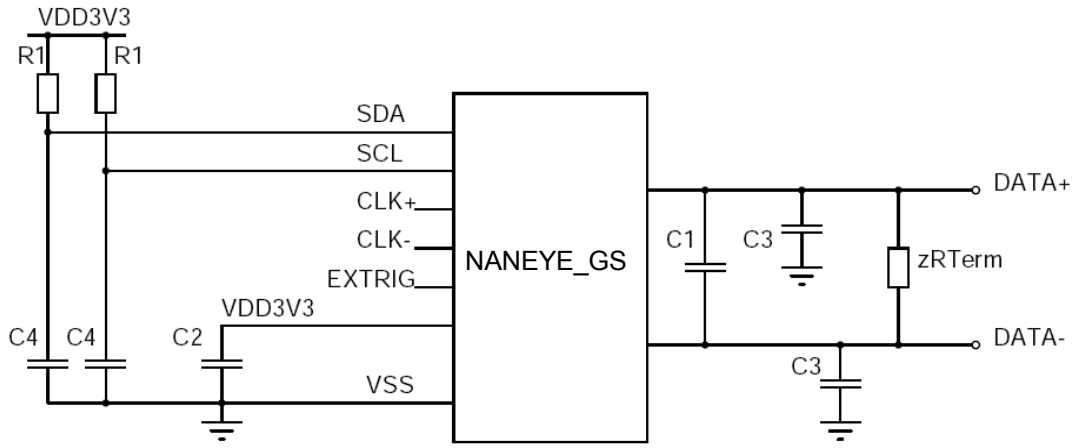

Figure 2: External Components

Component	*Description*	*Nominal Value*
C1	Differential load on LVDS lines	< 3pF
C2	Power supply decoupling	1uF // 1nF low ESR
C3	Single ended load LVDS lines	< 5pF
C5	Parasitic load SDA Line	< 50pF
zRterm	Impedance of LVDS termination	120 Ohm
R1	I2C pull up resistor	3k Ohm

Table 1: External components

9 Electrical Description

The sensor will comply to the specifications listed in this section within the operating ranges listed in the respective section.

An applied signal must not have a deviation from the ideal signal, at the pin of the circuit, such that the circuit or the parameter under test are affected significantly.

Proper decoupling of the circuit according to section is required. The following section defines the limits of functional operation and parametric characteristics of the circuit, and reliability. Note that functionality of the circuit outside the operating range as specified in this section is not guaranteed.

9.1 Absolute Maximum Ratings

Stresses above those listed in this clause may cause immediate and permanent device failure. Operation outside the operating conditions for extended periods may affect device reliability. It is not implied that more than one of these conditions can be violated simultaneously.

Symbol	*Description*	*Min*	*Max*	*Unit*
VDD3V3	Power supply voltage (analogue)	-0.5	3.6	V
VIO3V3	Voltage on any 3.3V IO	-0.5	3.6	V
Ta	Ambient temperature	-40	160	ºC

Table 2: Absolute Maximum Ratings

9.2 Electrical overstress immunity

The device withstands 500Volts ESD pulses when tested according to:

- HBM CDF-AEC-Q100-002/JESD22-A114/MIL STD 883 method 3015.7

9.3 Operating Conditions

Functional operation is guaranteed under these conditions.

Symbol	*Description*	*min*	*typical*	*max*	*unit*
VDD3V3	Power supply voltage (analogue)	3.0	3.3	3.6	V
VnrmsVDD3V3	RMS Noise on VDD3V3			5	mV
VnppVDD3V3	Peak to Peak Noise on VDD3V3			20	mV
FCLK	Input Clock Frequency	12.5	25	50	MHz
Duty_CLK	Input Clock Duty cycle	45	50	55	%
Jitter_CLK	Input Clock Jitter			200	ps
Cload	Load capacitance on digital outputs			15	pF
Ta	Ambient temperature*	-40	55	105(*)	ºC
Tj	Junction Temperature	-40	25	125	ºC
VIL	Low level input voltage	0	0.6	V	VIL
VIH	High level input voltage	2.6	3.6	V	VIH

Table 3: Operation Conditions

(*) - Digital functionality up to 120ºC

9.4 Electric Characteristics

9.4.1 LVDS OUTPUT

Symbol	*Description*	*Min*	*Max*	*Unit*
V_{CM}	Common Mode output voltage	0.9	1.1	V
V data+,data-	Absolute output voltage range	0.4	1.5	V
I data+,data-	LVDS output signal current (programmable range)	500	2000	uA
tslew, rising	Output slew rate of rising edge		1	ns
tslew, falling	Output slew rate of falling edge		1	ns

Table 4: Electric Characteristics

9.5 Optical Characteristics

Parameter	*Min*	*Typ*	*Max*	*unit*
Pixel Size/Pitch x	--	3.6	--	um
Pixel Size/Pitch y	--	3.6	--	um
Number of pixels in x direction	--	640	--	pixels
Number of pixels in y direction	--	640	--	pixels
Number of dark and test pixels x	--	4	--	pixels
Number of dark and test pixels y	--	0	--	pixels
Total number of light sensitive pixels	--	407040	--	pixels
DSNU rms			12	DN
PRNU rms			2	%
Responsivity at unity gain		12		$DN/nJ/cm^2$
Programmable exposure time (integration time)	8,96	-	167452	us
Full Well capacity		16		ke-
Total QE		39.5		%

Table 5: Optical Characteristics

10 Functional Description

10.1 General Sensor description

The outlined sensor is used for area scan applications with a high global shutter efficiency. The architecture permits 2 functional modes and 3 AD conversion resolutions. It is also possible to program the integration timing by configuring the pre-scale and integration time registers.

With respect to the response function there are available the following 2 response modes, set by the register configuration:

- Linear response.
- Piecewise linear response with compression of pixel response for higher light intensities.

With respect to AD conversion, a linear AD conversion of 10bit is implemented. The AD conversion is controllable such as to obtain the following additional AD resolution:

- Full linear 10 bits AD conversion
- Linear 9 bit AD conversion (1 bit reserved for validate data during the transmission)
- Linear 8 bit AD conversion (1 bit reserved for validate data and 1 bit reserved for LVAL during the output transmission)

There is a companding mode available that can be applied in the 3 AD conversion modes. When companding mode is selected the conversion step is doubled after a programmable threshold value is reached.

With respect to readout, the architecture sets a defined data rate, linearity dependent, of the main clock by a LVDS communication. The row addressing is done sequential to all rows leading to constant readout speed for the same main clock.

10.2 Interfaces

This sensor is configured by a serial interface communication and uses a LVDS standard communication to send the data out.

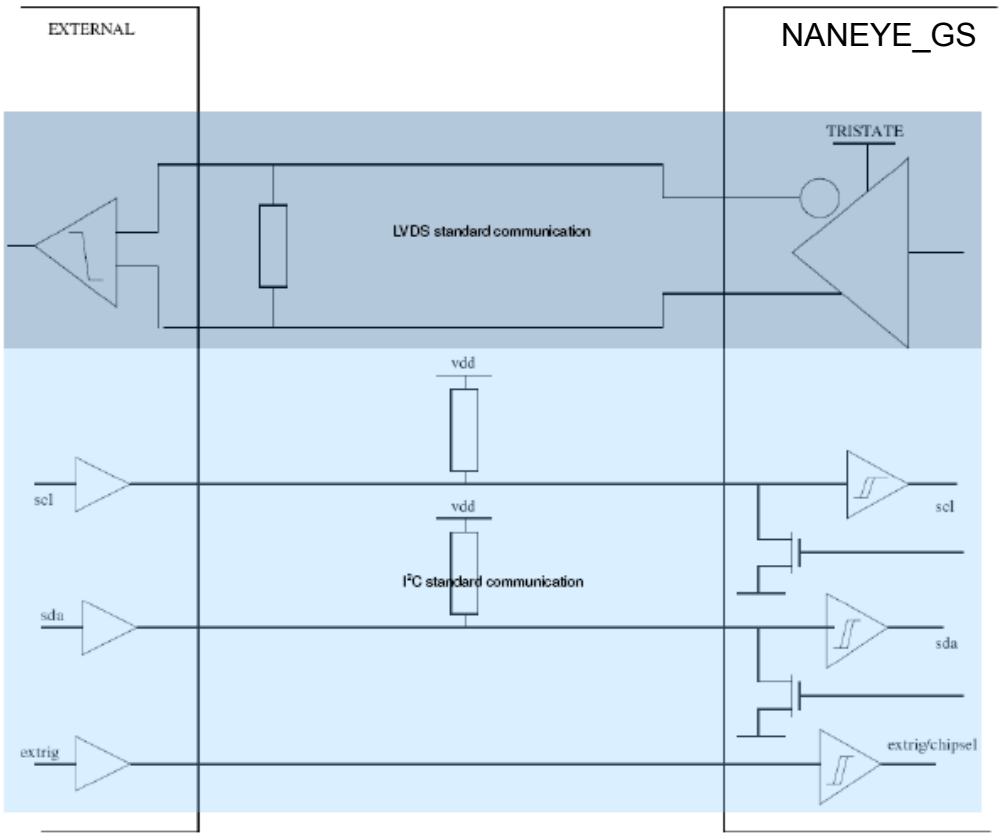

Figure 3: Types of communication interface

10.2.1 Serial Interface

The serial interface is implemented on a hardware level compatible to I2C interface hardware. The device ID is fixed for all devices of NANEYE_GS sensor. To share an interface bus for multi sensor applications, the serial communication is enabled by the device address and by a high level on the EXTRIG line. A falling edge of the EXTRIG line will update the shadow registers content to the effective registers and start the next exposure time counter.

NOTE: if interleaved shutter mode is selected, the pixel automatically starts the next integration with the start of readout, and remains in integration until the next end of the programmed integration time.

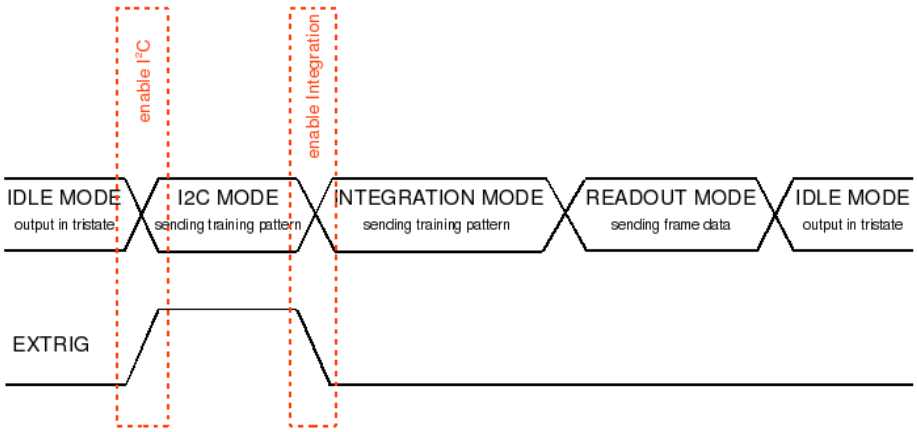

Figure 4: Extrig signal sensor control (Integration time indicated for non interleaved shutter mode).

For more detailed information got to chapter 11.1.1.

10.2.2 Data interface

The LVDS data interface is compatible to off the shelf deserializer components. Alternatively de serialization can be implemented in CPLD or FPGA components. The sensor data outputs are set in tristate during idle mode when data is not sent such that several sensors can be operated on the same data bus.

NOTE: For use of the sensor with stand alone deserializer components it is important to enable continuous data output by setting Register addres 0x01 bit 7 = 0.

10.3 Sequence of operation

The NANEYE_GS communication is performed according a sequence of the following different modes:

- IDLE MODE: during this mode the data+ and data- output are in tristate, so the communication data line is not hold by none of the sensors.
- CONFIGURATION (I2C) MODE: during this mode the external circuit is configuring one of the sensors using the serial communication signals (SCL and SDA). The addressed sensor will continue to send the training pattern during configuration mode. The falling edge of EXTRIG will validate the configuration data from the shadow registers to the effective registers.
- INTEGRATION: during this mode the sensor stops the serial communication and starts integration according with the configuration previously done. During this mode the sensor is still sending the training pattern.
- READOUT: during this mode the sensor assumes that the synchronism is done and replaces the training pattern by the image data pattern. Although IDLE, CONFIGURATION (I2C) and INTEGRATION modes duration time are set by user, the READOUT mode has always the same number of main clocks -> 499840 MCLK (781MCLK * 640rows). This mode ends after all the frame have been readout passing again to idle mode.

NOTE: if interleaved shutter mode is selected, the pixel automatically starts the next integration with the start of readout, and remains in integration until the next end of the programmed integration time.

In order to enable maximum sharing of data and configuration bus lines, the sequence of operation for the NANEYE_GS sensors follows the following sequence of mode states.

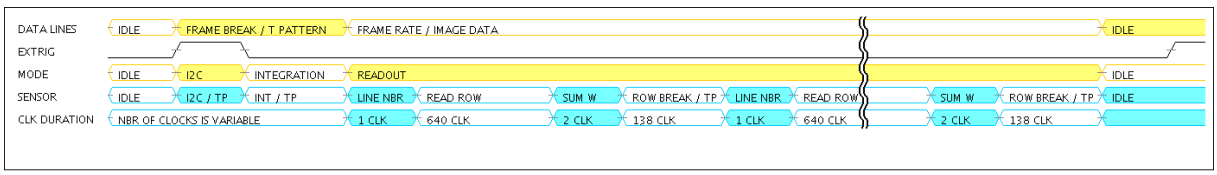

Figure 5: Operation states sequence for NANEYE_GS sensor

10.4 Timing characteristics

The timing characteristics for the NANEYE_GS sensor were determined according the required number of frames per second.

This sensor is able to work in 3 different frame rates:

- 100 FPS – using a main clock of 50MHz
- 50 FPS – using a main clock of 25MHz
- 25 FPS – using a main clock of 12.5MHz

Note that is also possible to use the 50Mhz as the input reference main clock and to change the Frame rate by register.

Different frame rate / frame period will lead to different row period:

- 100FPS => 15.62us (781 clocks / 50MHz)
- 50FPS => 31.24us (781 clocks / 25MHz)
- 25FPS => 62.48us (781 clocks / 12.5MHz)

From the 781 main clocks only 640 are for pixel data readout, the others clocks are for:

- identify the number of line - 1 clock
- the error detection word - 2 clock that does the parity check number
- the sending training pattern - 138 clock.

10.5 Data sequence and line transmission

In order to provide a high degree of data integrity each line is transmitted between a line number and a sum word of 24 bits. This word is for errors detection during transmission from the sensor to the receiver. In order to ease de-serialization prior to each frame and in the line brake a training pattern is transmitted.

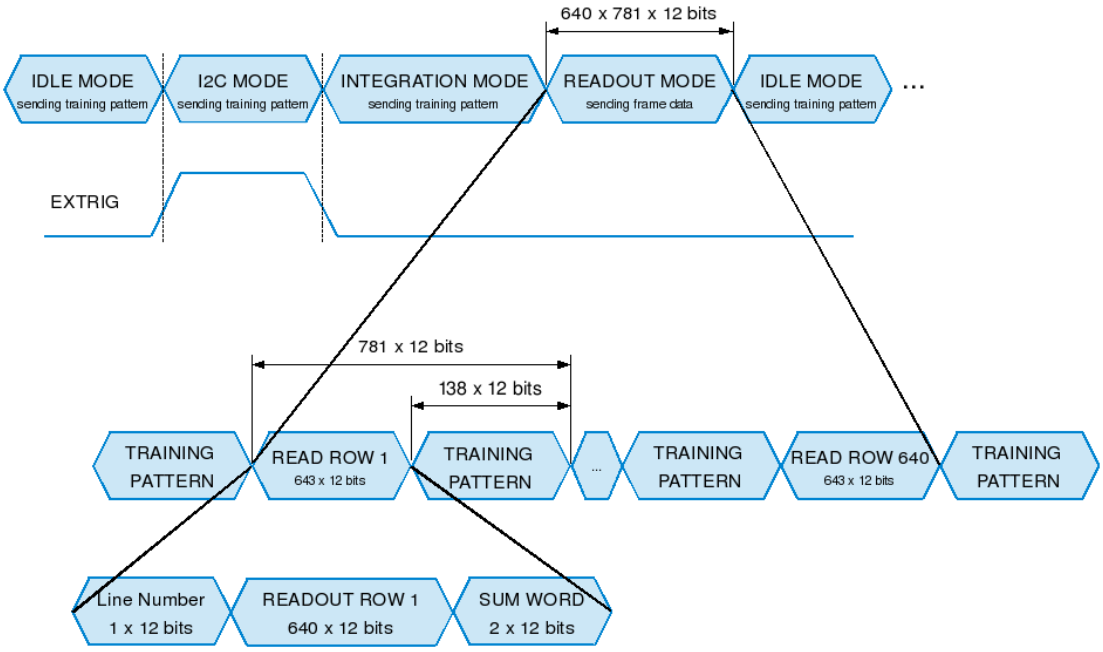

Figure 6: Data sequence and content of a line transmission

Training pattern is transmitted after detection of EXTRIG signal at “high”, what means that it will be transmitted during I2C mode and integration mode. In readout training pattern transmission is swapped with data from each row. In readout the transmission is always of 640x781x12 bits where 640 corresponds to the number of rows in sensor, 781 corresponds to the number of transmitter data needed for read one row and the 12 bits are the word size. The transmitter data is divided in 138 training pattern and 643 data words, which has 1 word for the line number, 640 for each column to complete one row and 2 word for error detection word.

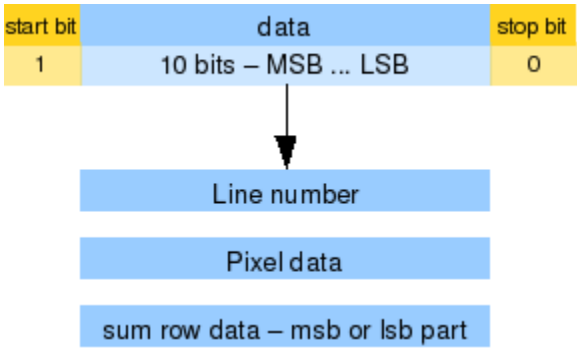

Figure 7: word data

The data words have one start bit followed by 10 bits (MSB to LSB) and are ending with a stop bit. The different is only in the type of information sent in the 10 reserved bits. Note that each sum word is transmitting part of the pixel row data sum, in the first sum word is sent the MSB and the LSB are sent in the second.

The 2 words sent for error detection represent the sum of each data row, can be processed outside according cryptographic hash functions or cyclic redundancy checks schemes.

The Sensor interface is compatible with many off the shelf de-serialization IC's that translate a 12:1 bit serial stream in a 10bit parallel stream.

NOTE: For use of the sensor with stand alone deserializer components it is important to enable continuous data output by setting Register address 0x01 bit 7 = 0.

10.6 Multiple sensor application scenarios

10.6.1 Option 1

Use of shared LVDS bus and off the shelf deserializer, sequential triggering of the sensors and combining to “super frame” in control unit.

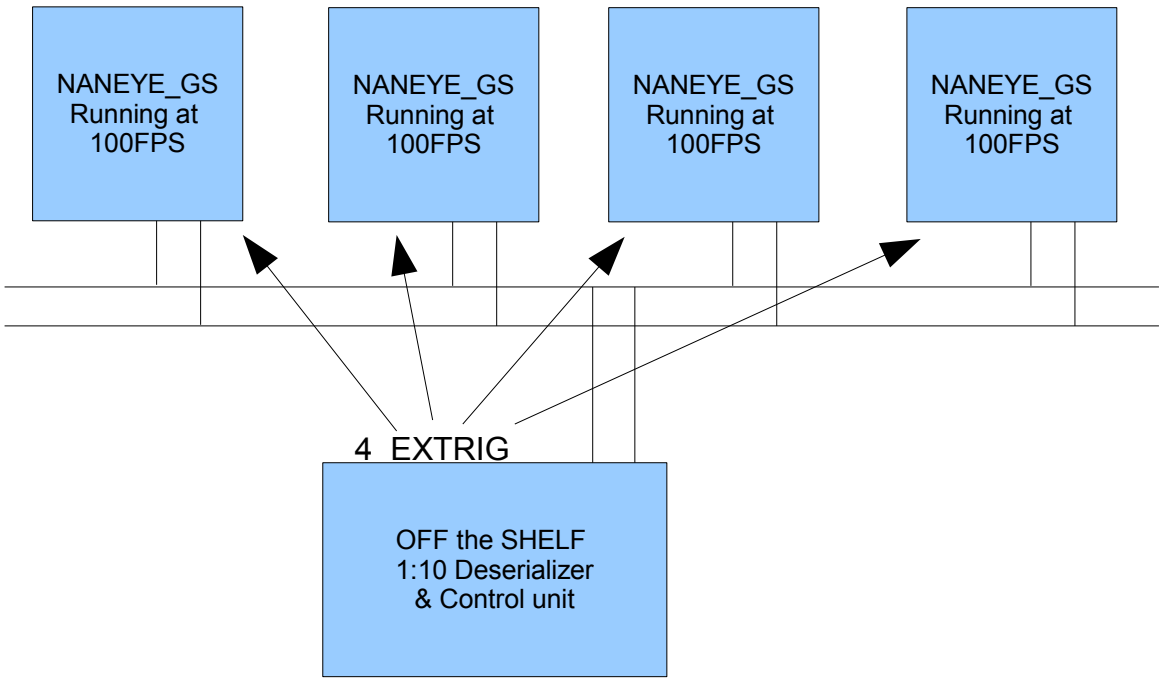

Figure 8: Multiple sensor application with shared LVDS data bus

10.6.2 Option 2

Use of custom CPLD based de serialization application for pixel synchronous sensor operation and memory free image combination. (note: Extrig needs to be routed individually in order to program separate integration times in different sensors.)

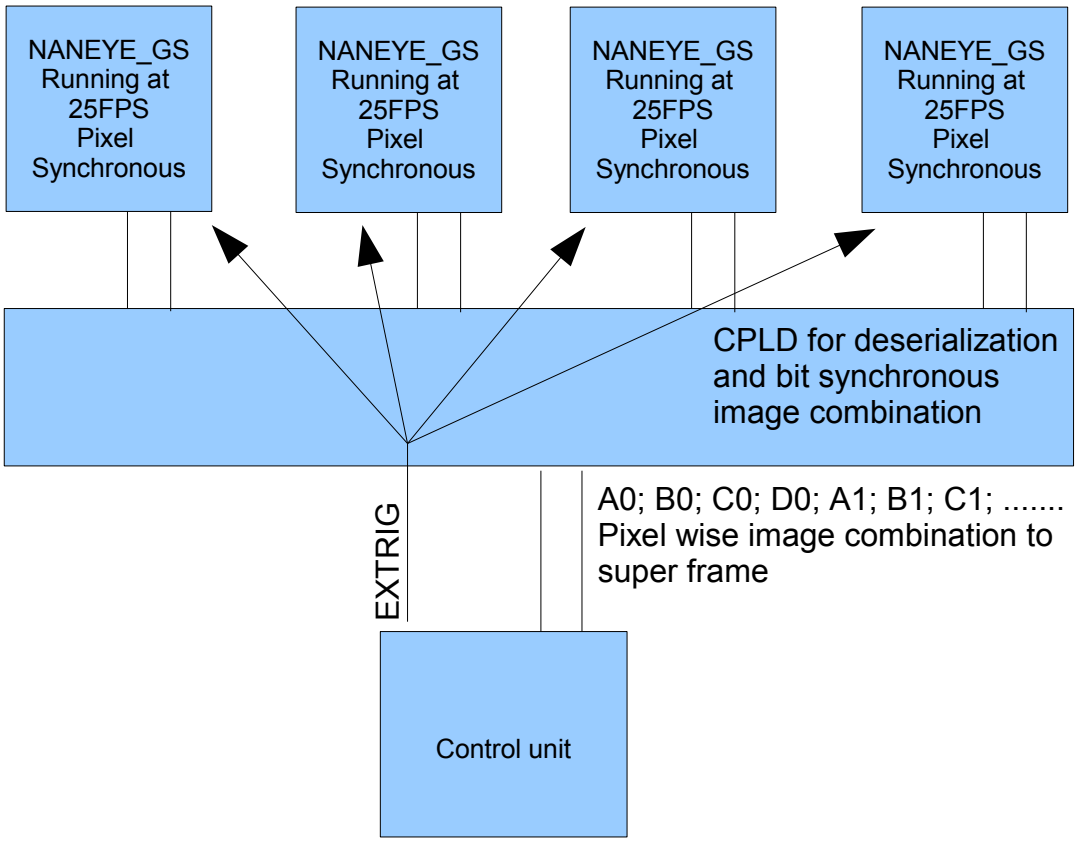

Figure 9: Multiple sensor application with memory buffer free image combination

11 Control Interface

11.1.1 Serial Interface (I^2C similar)

Although the compatible with the I2C interface the sensor is only set to work as slave. So according this, it can work in two modes: slave-receiver or a slave-transmitter.

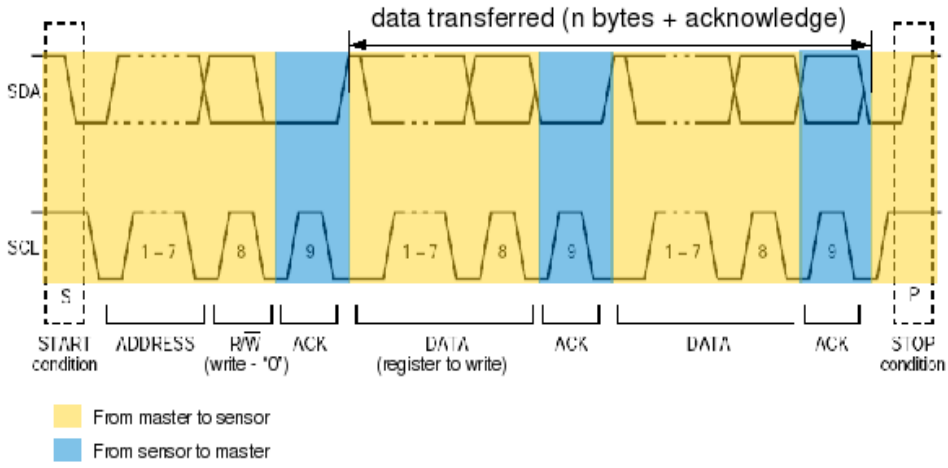

Figure 10: Master-transmitter writing for a slave receiver.

In slave-receiver mode:

- first data is used for define the register to be written
- next data is the content for the previously defined register

The master must be aware that before sending data is necessary to identify the register to be written. Sensor will be responsible for pull down the SDA line during the acknowledge clock pulse.

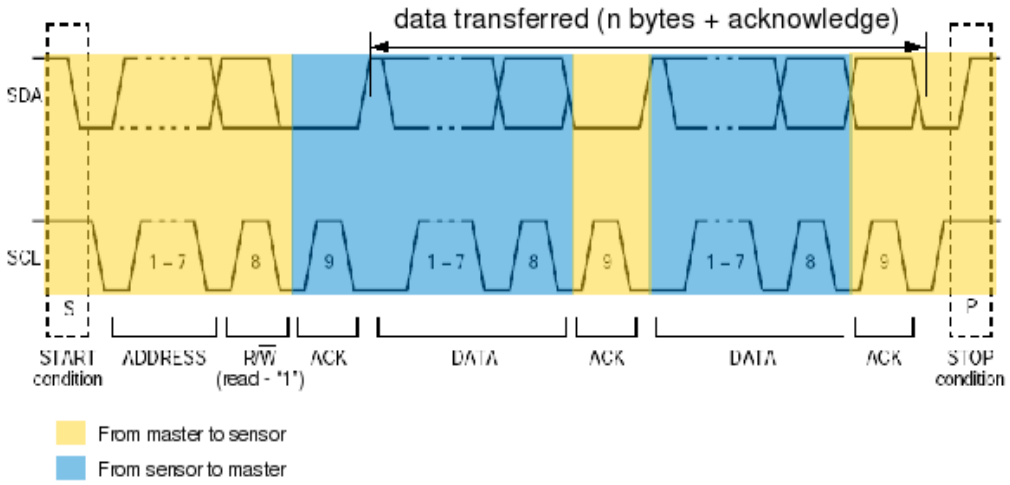

Figure 11: Master-transmitter reading from a slave receiver.

In slave-transmitter mode:

- sensor will read all registers in burst mode but will stop communication if does not receive an acknowledge by the master.

The master must be aware that it cannot set which register to read, it reads in burst mode. Sensor will release the SDA line to "high" during the acknowledge clock pulse.

The sensor can also hold the clock line SCL "low" to force the master into a wait state if by some reason it cannot receive or transmit the byte of data (FEATURE NOT APPLIED).

I2C hard wired values:

SI_ID[7:0] – I2C Bus Device Address

	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 3**	**Bit 1**	**Bit 0**
Description	SI_ID[7]	SI_ID[6]	SI_ID[5]	SI_ID[4]	SI_ID[3]	SI_ID[2]	SI_ID[1]	SI_ID[0]
Value	1	0	1	1	0	0	0	0

SI_NBR_REG[7:0] – Number of registers of the device

	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 3**	**Bit 1**	**Bit 0**
Description	SI_NBR_ REG[7]	SI_NBR_ REG[6]	SI_NBR_ REG[5]	SI_NBR_ REG[4]	SI_NBR_ REG[3]	SI_NBR_ REG[2]	SI_NBR_ REG[1]	SI_NBR_ REG[0]
Value	0	0	0	1	0	0	0	0

12 Pinout

12.1 Pads and Bond Pads position

Below is presented the internal pads and bond pads placement as the correspondent routing. (**Top View means looking on (resp. through) the device from the pixel side. Such as the light is impinging through the lens on the sensor**). This result in the same view as the layout on a receiving PCB top layer should be.

The position of the pixel matrix is central to the device with a nominal spacing of 548um to each edge of the component.

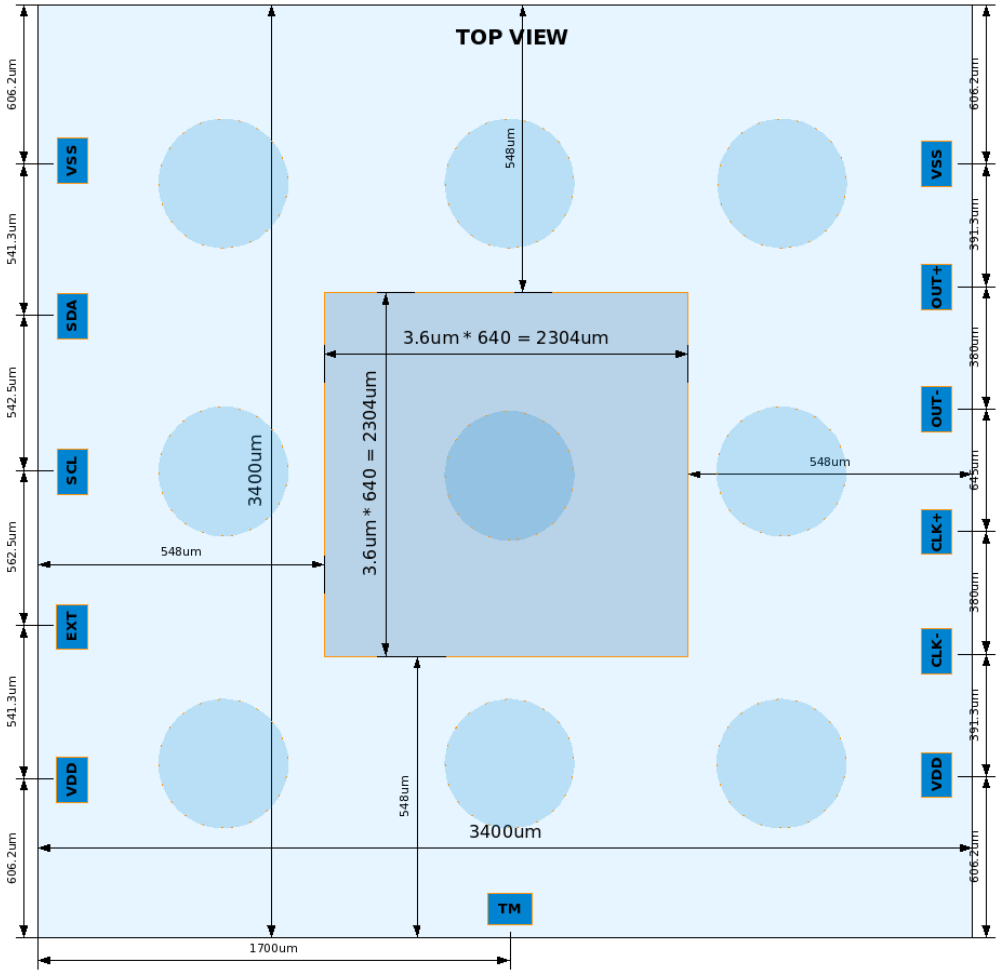

Figure 12: Pads placement (Top View)

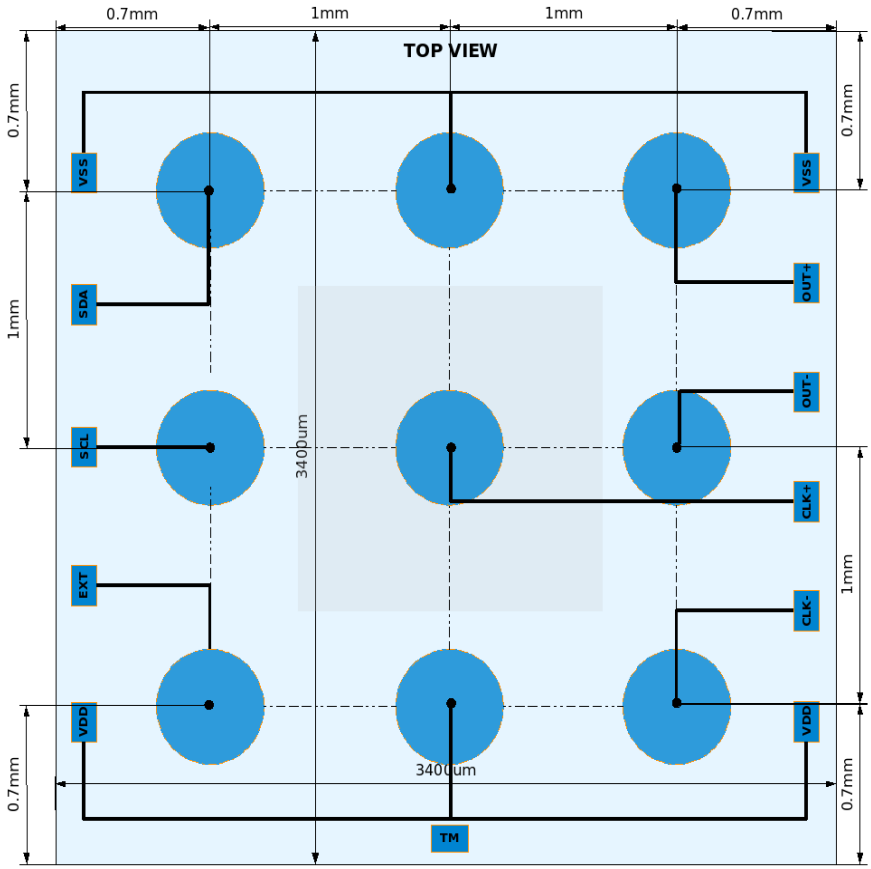

Figure 13: Bondpads placement and connection with internal pads (Top View)

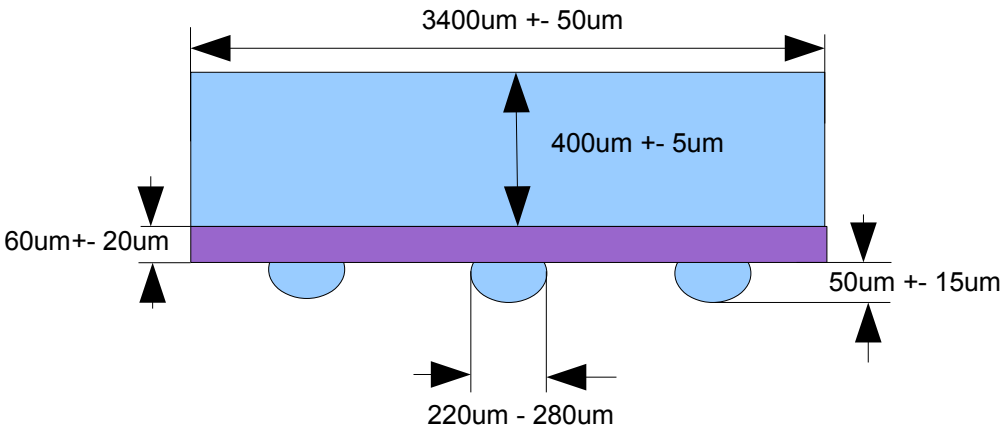

Figure 14: Side view of BGA package

12.1.1 Pin Coordinates

Nbr	*Pad Name*	*Function/Type*	*x[um]*	*y[um]*
			SOLDER BUMP	*SOLDER BUMP*
1	SDA	Bidirectional Analogue 3.3V	700	2700
2	SCL	Bidirectional Analogue 3.3V	700	1700
3	EXT	EXTRIG signal input	700	700
4	VDD	Supply Analogue 3.3V	1700	700
5	VSS	Ground	1700	2700
6	CLK+	Clock Differential Signal Input	1700	1700
7	CLK-	Analogue 3.3V	2700	700
8	OUT+	LVDS Differential Signal output	2700	2700
9	OUT-	Analogue 3.3V	2700	1700

Note:

Origin lower left corner in “Top View”.

End of Document